POWER REDUCTION CIRCUIT AND METHOD
WITH MULTI CLOCK BRANCH CONTROL
Sinclair, et al. 09/325,882

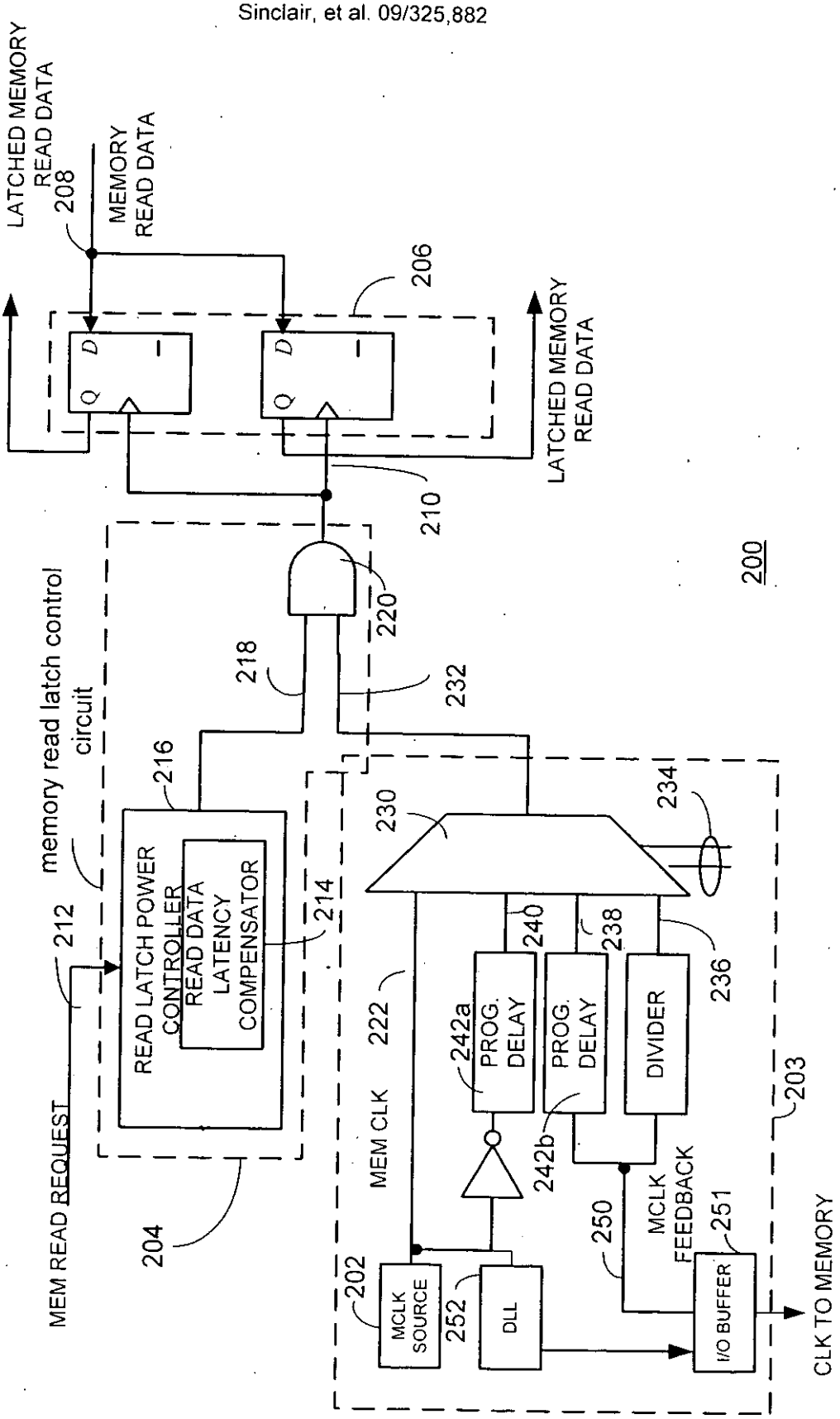


FIG. 2

POWER REDUCTION CIRCUIT AND METHOD
WITH MULTI CLOCK BRANCH CONTROL
Sinclair, et al. 09/325,882

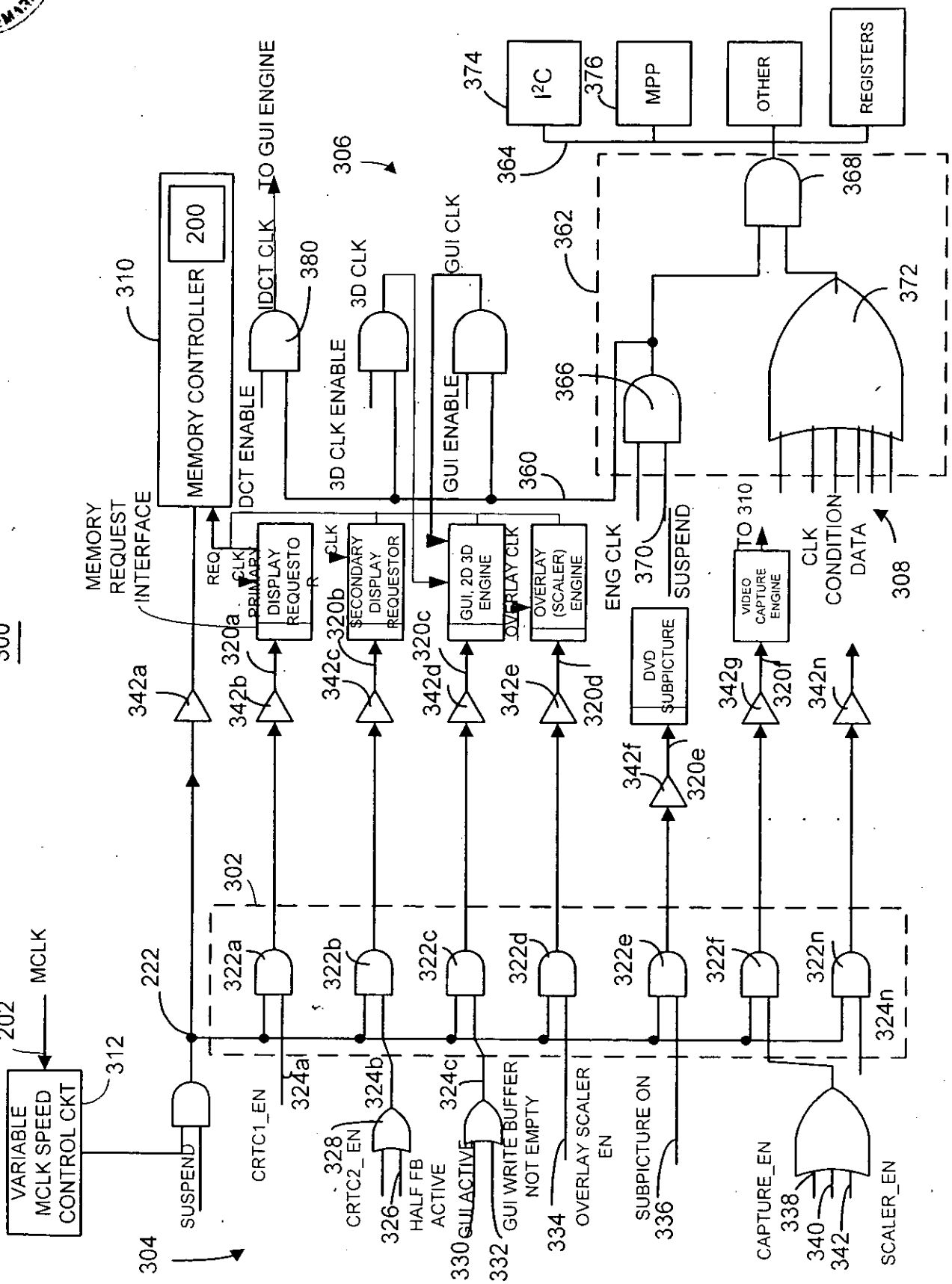
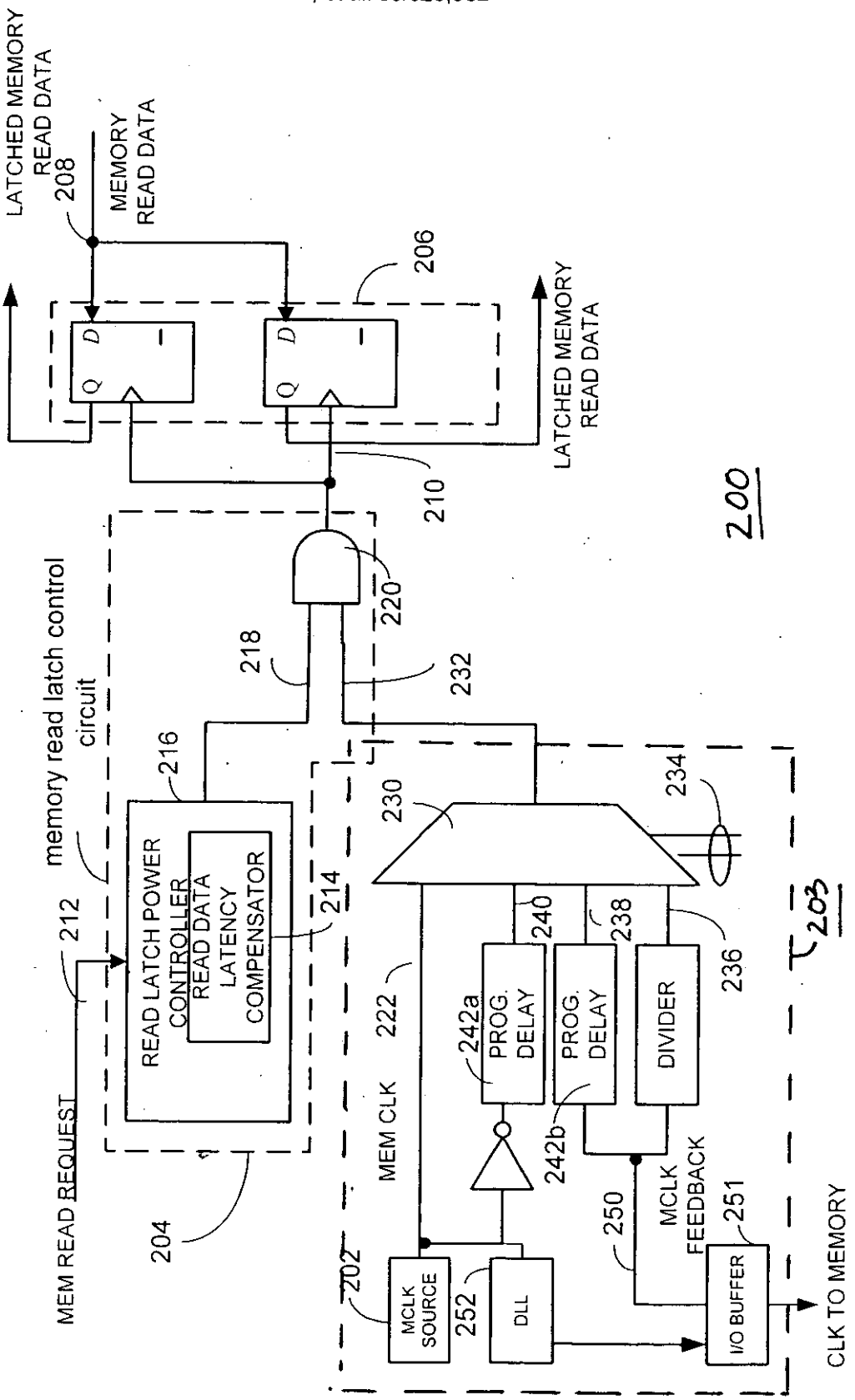


FIG. 3

POWER REDUCTION CIRCUIT AND METHOD
WITH MULTI CLOCK BRANCH CONTROL
Sinclair, et al. 09/325,882



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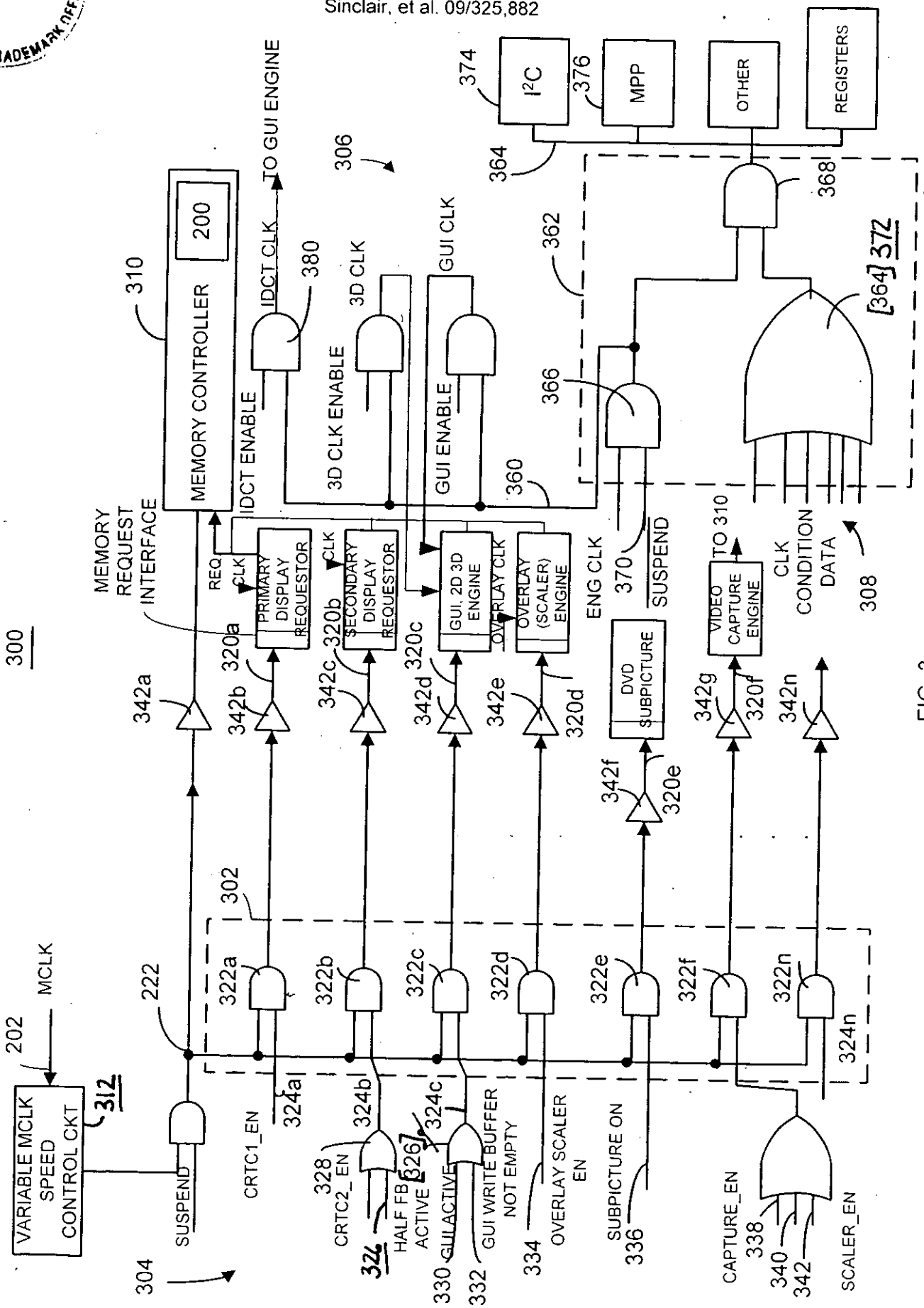

FIG. 3